**Amendments to the Specification:**

Please replace the paragraph beginning on page 1, line 7 with the following amended paragraph:

Frequency conversion is the process of changing one frequency to another. This may occur in instances when one signal is multiplied with a second signal to produce[[,]] a sum and/or difference of the signals. Frequency conversion circuits are commonly used in transmitters/receivers to convert an outgoing/incoming Intermediate Frequency/Radio Frequency (IF/RF) signal to the RF/IF signal. In case of receivers the IF signal is further processed by circuits following the frequency conversion circuit to develop a suitable signal for passing to a demodulator. The demodulator recovers the information encoded into the IF signal. The frequency conversion circuit produces the IF signal by mixing the RF signal with one or more local oscillator (LO) signals using a mixer.

Please replace the paragraph beginning on page 3, line 7 with the following amended paragraph:

Implementations of the above aspect may include one or more of the following. The means for generating a low-interference clock further includes means for generating an asymmetrical clock signal. The means for changing the duty cycle further comprises means for changing the position of the falling edge of the square wave clock relative to the position of the rising edge of the clock. ~~The~~ Minimizing of the nth-order harmonic changes the magnitude of other harmonic. The low-interference clock can be used in a digital radio transceiver.

Please replace the paragraph beginning on page 4, line 6 with the following amended paragraph:

Implementations of the above aspect may include one or more of the following: The clock oscillator generates an output at a high frequency relative to the desirable low frequency clock rate. The counter is a modular down counter. The controller can change the position of the falling edge of the clock relative to the position of the rising edge of the clock. The controller can minimize the nth-order harmonic and change[[s]] the magnitude of other harmonic.

Please replace the paragraph beginning on page 9, line 1 with the following amended paragraph:

FIG. 3 shows an exemplary process that minimizes or eliminates nth-order harmonic, particularly nth-order harmonic associated with a square wave clock signal having a predetermined frequency and a duty cycle. The process includes changing the duty cycle of the clock to eliminate or suppress the nth-order harmonic of that clock (step 12). Next, a low-

interference clock having the changed duty cycle while keeping the predetermined frequency is generated (step 14). The low-interference clock can be an asymmetrical clock signal. Since the square wave clock has rising and falling edges, the changing of the duty cycle changes the position of the falling edge of the square wave clock with respect to the position of the rising edge of the clock.